REMARKS/ARGUMENTS

Reconsideration and allowance are respectfully requested. No new matter has been added by the amendments herein.

Claim Rejections

Claims 1, 3-9, 11, and 13-15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,781,799 to Leger, et al. ("Leger") in view of U.S. publication no. 2003/0033454 A1 to Walker et al. ("Walker"), and further in view of U.S. Patent No. 6,691,178 to Kasper ("Kasper"). Applicant respectfully traverses this rejection.

Independent Claim 1

Independent claim 1 recites:

> coupling said respective DMA modules over a data transfer facility in a chain arrangement where each DMA module, other than the last in the chain, has its respective output buffers coupled to the input buffer of another of said DMA modules downstream in the chain and each of said DMA modules, other than the first in the chain, has its respective input buffer coupled to the output buffer of another of said DMA modules upstream in the chain….

Leger

The Office Action compares the recited DMA modules with DMA controllers 20 of Leger (Fig. 2). However, as conceded by the Office Action, Leger fails to teach or suggest coupling input and output buffers of DMA modules in a chain, as recited in claim 1.

Leger plus Walker

Instead, the Office Action alleges that it would have been obvious to modify Leger to incorporate input and output buffers that are allegedly part of the multi-port DMA 5 of Walker (Fig. 2) into each of the DMA controllers 20 of Leger, so as to facilitate coupling between DMA modules. The alleged motivation for modifying Leger would be to enable other modules to access the system bus while a DMA controller is handling a transfer between two modules (referring to Walker at paragraph 5, lines 2-6).

It is respectfully submitted that the Office Action is misinterpreting Walker, and in particular may be confusing the term "module" with "DMA controller" as used in Walker. Walker at paragraph 5 is not concerned with transferring data between two DMA controllers, as alleged by the Office Action, but rather it discusses the problems that arise when a DMA controller handles a transfer between two "modules," or locations. See also Walker paragraphs 0009 and 0011, which discuss how a DMA controller can perform a data transfer between two locations, such as a processor, memory, or bus, without occupying the system bus. In this case, there is nothing to teach or suggest that the two modules, or locations, are two DMA controllers that are communicating with each other.

Thus, even if Leger were somehow modified with the buffers of Walker as proposed, this would still not result in a system where two "DMA controllers" (the term used in Walker) or two "DMA modules" (the term used in claim 1) would be able to communicate with each other at all.

Moreover, it can now be seen that the alleged reason for modifying Leger with Walker (to facilitate coupling between two DMA modules) is not supported by either Leger or Walker.

Leger plus Walker, plus Kasper

The Office Action further concedes that the combined Leger-Walker system would still fail to have the various DMA controllers chained together as claimed. Instead, the Office Action relies on Kasper to teach chaining the DMA controllers of Leger-Walker together. In doing so, the Office Action alleges that Kasper discloses that associated entries (descriptors) in a descriptor ring are chained together at col. 3, lines 9-10. Even so, the entries/descriptors are not the DMA controllers, or buffers, or in fact any element of the system at all. Rather, descriptors are merely data that is stored in the buffers. Thus, the teaching that descriptors (i.e., data) may be chained together, or that such data may span multiple buffers, has nothing to do with actually chaining together the input and output buffers of DMA controllers as claimed.

Moreover, if the Office Action is attempting to compare the recited DMA modules with HDLC ports 50-56 of Kasper in Fig. 2, and somehow alleging that these HDLC ports are chained together, then this is a flawed comparison. The HDLC ports 50-56 are ports within a single network controller 40. Kasper, col. 5, lines 22-23 ("As shown in FIG. 2, on the network side, the network controller 40 contains four ports 50, 52, 54, and 56…."). And, if the Office Action is comparing each network controller 40 of Fig. 1 with a different DMA module as claimed, then

there is nothing in Kasper to teach or suggest chaining together the various network controllers 40 in the manner claimed.

Conclusion

As explained above, neither Walker nor Kasper provide for chaining of DMA modules as claimed, and thus modifying Leger with these still fails to provide a system of such chained DMA modules. For at least these reasons, it is submitted that claim 1 is allowable over Leger, Walker, and Kasper, either alone or in combination.

Independent Claims 5 and 11

Independent claims 5 and 11 are also allowable over Leger, Walker, and Kasper for at least similar reasons as discussed above with regard to claim 1.

Dependent Claims

The dependent claims are also allowable by virtue of depending from allowable independent claims, and further in view of the additional features recited therein.

Conclusion

All rejections having been addressed, Applicant respectfully submits that the present application is in condition for allowance, and respectfully solicits prompt notification of the same. Should the Examiner have any questions, the Examiner is invited to contact the undersigned at the number below.

Respectfully submitted,

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